

PCT

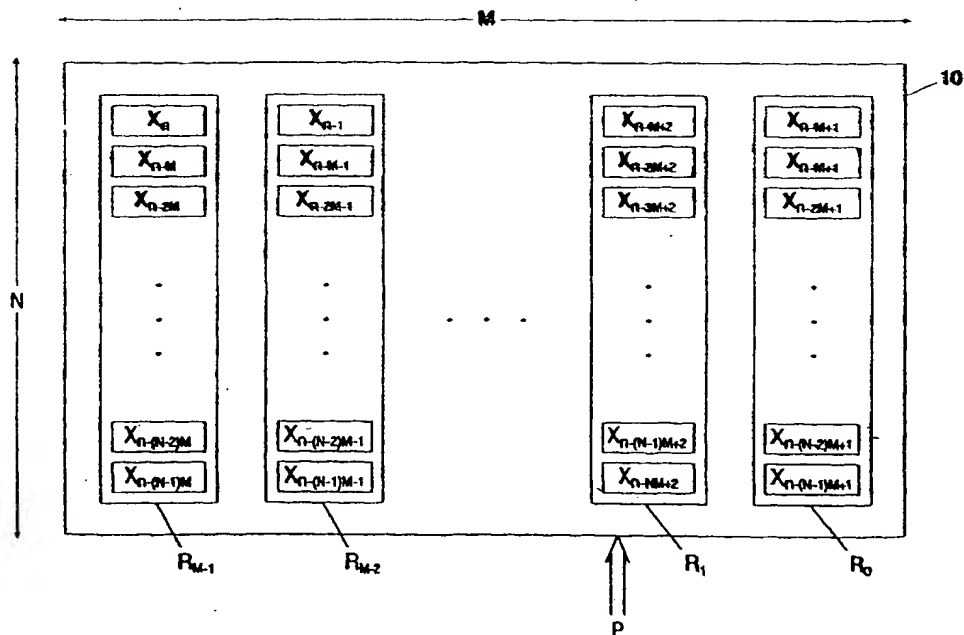
WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : G06F 9/455	A1	(11) International Publication Number: WO 99/19798
		(43) International Publication Date: 22 April 1999 (22.04.99)
(21) International Application Number: PCT/US98/19708 (22) International Filing Date: 18 September 1998 (18.09.98) (30) Priority Data: 08/947,467 9 October 1997 (09.10.97) US (71) Applicant (for all designated States except US): I.C. COM LTD. [IL/IL]; Hashikma 3, 58001 Azor (IL). (71) Applicant (for TJ only): FRIEDMAN, Mark, M. [US/IL]; Alharizi 1, 43406 Raanana (IL). (72) Inventor; and (75) Inventor/Applicant (for US only): MOLEV-SHTEIMAN, Arkady [IL/IL]; Abba Hillel Silver 57A/4, 52532 Ramat Gan (IL). (74) Common Representative: FRIEDMAN, Mark, M.; c/o Castorina, Anthony, Suite 207, 2001 Jefferson Davis Highway, Arlington, VA 22202 (US).		(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published <i>With international search report.</i> <i>Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>

(54) Title: METHOD OF EMULATING A SHIFT REGISTER USING A RAM



(57) Abstract

A method using a RAM (10) and a short shift register (20) to emulate a long shift register to store a stream of incoming bits. A pointer points to one of the RAM registers. To store an incoming bit, the contents of the RAM register pointed to by the pointer are written to the shift register (20) and shifted by one bit, the incoming bit is stored in the location in the shift register (20) freed up by the shift operation, the updated contents of the shift register (20) are written back to the RAM register pointed to by the pointer, and the pointer is incremented.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece			TR	Turkey
BG	Bulgaria	HU	Hungary	ML	Mali	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MN	Mongolia	UA	Ukraine
BR	Brazil	IL	Israel	MR	Mauritania	UG	Uganda
BY	Belarus	IS	Iceland	MW	Malawi	US	United States of America
CA	Canada	IT	Italy	MX	Mexico	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NE	Niger	VN	Viet Nam
CG	Congo	KE	Kenya	NL	Netherlands	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NO	Norway	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	NZ	New Zealand		
CM	Cameroon			PL	Poland		
CN	China	KR	Republic of Korea	PT	Portugal		
CU	Cuba	KZ	Kazakstan	RO	Romania		
CZ	Czech Republic	LC	Saint Lucia	RU	Russian Federation		
DE	Germany	LI	Liechtenstein	SD	Sudan		
DK	Denmark	LK	Sri Lanka	SE	Sweden		
EE	Estonia	LR	Liberia	SG	Singapore		

METHOD OF EMULATING A SHIFT REGISTER USING A RAM

5 FIELD AND BACKGROUND OF THE INVENTION

The present invention relates to digital computation and, more particularly, to a method of emulating a very long shift register, using a random access memory (RAM) and a short shift register.

There are many applications in which a stream of incoming bits must be
10 processed in real time. For example, it may be desired to apply a finite impulse response filter, each of whose coefficients is a single bit, to a stream of incoming bits. Denoting the K coefficients of the filter as $\{C_k\}$ ($k=0$ through $K-1$) and the bits of the input stream (of indefinite length) as $\{X_n\}$, this means that the output of the filter is a set of numbers $\{Y_n\}$ such that

$$15 \quad Y_n = \sum_{k=0}^{K-1} C_k X_{n-k}$$

and the indicated operation is an XOR operation.

The straightforward way to implement this filter would be to provide a register of length K to store the coefficients $\{C_k\}$ and a shift register of length K bits to store sequences of input bits $\{X_n\}$. As each new input bit arrives, the contents of the shift
20 register are shifted over one bit to accommodate the new input bit. Note that this automatically discards the old input bit that preceded the new input bit by K bits. In-between arrivals of new input bits, an inner product operation is performed on the contents of the coefficient register and the shift register, to obtain the latest filter output.

This straightforward implementation suffers from the drawback that for filters of a useful length (for example, $K=1024$), a correspondingly long shift register is prohibitively expensive to fabricate on a processor chip. There is thus a widely recognized need for, and it would be highly advantageous to have, a method of
5 emulating a shift register using a less expensive form of memory, such as RAM.

SUMMARY OF THE INVENTION

According to the present invention there is provided a method of processing successive input bits, including the steps of: (a) providing: (i) a RAM having a
10 plurality of registers, each of the registers storing a word, all of the words being of equal length, (ii) a shift register at least as long as any of the words, and (iii) a pointer; (b) initializing the pointer to point to one of the registers of the RAM; and (c) for each group of j input bits: (i) writing the word, stored in the register pointed to by the
pointer, to the shift register, (ii) shifting the word in the shift register by j bits, (iii)
15 writing the group of j input bits to the shift register, thereby producing an updated word in the shift register, (iv) storing the updated word in the register pointed to by the pointer, and (v) incrementing the pointer.

A RAM typically consists of a group of individually addressable registers, each with a unique address, and in each of which a word of a certain length (typically
20 8, 16, 32 or 64 bits) may be stored and subsequently retrieved. The key to the present invention is the use of such a *word*-addressable memory to efficiently store successive individual input *bits* as they arrive. This is accomplished by also providing a relatively short (one word long) shift register and a pointer that encodes the addresses

of the RAM registers. The pointer is initialized to point to one of the RAM registers. As each input bit arrives, the word stored in the RAM register pointed to by the pointer is written to the shift register, shifted over one bit to make room for the new input bit, and written back to the RAM register whence it was retrieved. The pointer
5 then is incremented to point to the next RAM register. Note that "incrementing" the pointer is defined herein cyclically: incrementing a pointer that points to the last RAM register produces a pointer that points to the first RAM register. Note that the input bits are stored in the RAM in transposed order, as explained more fully below.

10 BRIEF DESCRIPTION OF THE DRAWINGS

The invention is herein described, by way of example only, with reference to the accompanying drawings, wherein:

FIG. 1 is an illustration of a RAM at the beginning of an incoming bit storage cycle;

15 FIGS. 2A and 2B are illustrations of an N-bit shift register at two different stages of an incoming bit storage cycle;

FIG. 3 is an illustration of a RAM at the end of an incoming bit storage cycle.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

20 The present invention is of a method of emulating a very long shift register, using a RAM. Specifically, the present invention can be used to apply a finite-impulse-response filter to a sequence of bits, and to transpose a sequence of bits.

The principles and operation of shift register simulation according to the present invention may be better understood with reference to the drawings and the accompanying description.

Referring now to the drawings, Figure 1 shows a RAM 10 with M RAM registers, indexed R_0 through R_{M-1} , each capable of storing N bits, for a total capacity of NM bits, at a moment in time when NM bits X_n through X_{n-NM+1} of an incoming bit stream have been stored according to the present invention. The incoming bit which arrived earliest, X_{n-NM+1} , is stored in the $(N-1)$ -th position in RAM register R_0 , the incoming bit which arrived next, X_{n-NM+2} , is stored in the $(N-1)$ -th position in RAM register R_1 , and so on. The most recently arrived bit, X_n , is stored in the 0-th position in RAM register R_{M-1} . A pointer P points to the RAM register, R_0 , that holds the earliest arriving stored incoming bit, X_{n-NM+1} , in its $(N-1)$ -th position.

The arrival of the next incoming bit, X_{n+1} , initiates the next incoming bit storage cycle. The first step is to write the contents of the RAM register, R_0 , pointed to by pointer P , to an N -bit shift register 20. Figure 2A shows N -bit shift register 20 at the end of this step. The second step is to shift the bits in N -bit shift register 20 up one position, discarding bit X_{n-NM+1} and making room in the 0-th position of N -bit shift register 20 for new incoming bit X_{n+1} . The third step is to store new incoming bit X_{n+1} in the 0-th position of N -bit shift register 20. Figure 2B shows N -bit shift register 20 at the end of this step. The fourth step is to write the contents of N -bit shift register 20 to the RAM register, R_0 , pointed to by pointer P . Finally, pointer P is incremented to point to RAM register R_1 , which now is the RAM register which now holds the

earliest arriving stored incoming bit, X_{n-NM+2} , in its $(N-1)$ -th location. Figure 3 shows RAM 10 at the end of this step.

In-between incoming bit storage cycles, the contents of RAM 10 may be read and manipulated in the conventional manner. For example, to produce the next output, Y_{n+1} , of the finite input response filter discussed above (assuming that $K=NM$), the M words stored in RAM 10 are successively read and XOR-ed with the coefficients $\{C_k\}$, which also are stored in M words in a different memory unit. Note that for this to be effected correctly, the coefficients $\{C_k\}$ must be stored in transposed order: $C_{K-1}, C_{K-M-1}, C_{K-2M-1}, \dots, C_{2M-1}, C_{M-1}, C_{K-2}, C_{K-M-2}, C_{K-2M-2}, \dots, C_{2M-2}, C_{M-2}, \dots$
 10 $C_{K-M+1}, C_{K-2M+1}, C_{K-3M+1}, \dots, C_{M+1}, C_1, C_{K-M}, C_{K-2M}, C_{K-3M}, \dots, C_M, C_0$. This is precisely the transposed order produced by applying the method of the present invention to the bits $\{C_k\}$, treating the bits $\{C_k\}$ as an incoming bit string.

Typical values of M and N are 32 and 32, respectively.

Pointer **P** is incremented cyclically. Thus, in the incoming bit storage cycle in which pointer **P** initially points to the highest-indexed register, R_{M-1} , "incrementing"
 15 pointer **P** means changing the value of pointer **P** to point to the lowest-indexed register, R_0 .

It will be appreciated that the principles of the present invention also are applicable to the processing of a stream of incoming bits other than one bit at a time. For example, the incoming bit stream may be processed three bits at a time, using
 20 RAM registers whose lengths are a multiple of 3 bits, and shifting the contents of the shift register by three bits in every incoming 3-bit storage cycle. The shift register must be at least as long as the RAM registers; if the shift register is used only for

unloading and loading the RAM registers, and the output of the shift register is not used in any other processing, then the length of the shift register need not be a multiple of 3 bits. The only practical limitation is that if bits are processed in groups of j , where j is a typical word length of a conventional RAM (for example, 8, 16 or 5 32), then the processing may as well be done word-wise rather than bit-wise, as described, for example, in U. S. Patent No. 5,568,443, to Dixon et al., in the context of the prior art.

While the invention has been described with respect to a limited number of embodiments, it will be appreciated that many variations, modifications and other 10 applications of the invention may be made.

WHAT IS CLAIMED IS:

1. A method of processing successive input bits, comprising the steps of:
 - (a) providing:
 - (i) a RAM having a plurality of registers, each of said registers storing a word, all of said words being of equal length,
 - (ii) a shift register at least as long as any of said words, and
 - (iii) a pointer;
 - (b) initializing said pointer to point to one of said registers of said RAM; and
 - (c) for each group of j input bits:
 - (i) writing said word, stored in said register pointed to by said pointer, to said shift register,
 - (ii) shifting said word in said shift register by j bits,
 - (iii) writing said group of j input bits to said shift register, thereby producing an updated word in said shift register,
 - (iv) storing said updated word in said register pointed to by said pointer, and
 - (v) incrementing said pointer.
2. The method of claim 1, wherein j equals 1.

3. The method of claim 1, wherein all of said registers of said RAM are as long as each of said words.

4. The method of claim 1, wherein said shift register is as long as each of said words.

5. The method of claim 1, further comprising the step of:

(d) successively reading and processing at least some of said words stored in said registers of said RAM.

6. The method of claim 5, wherein all of said words stored in said registers of said RAM are read successively and processed.

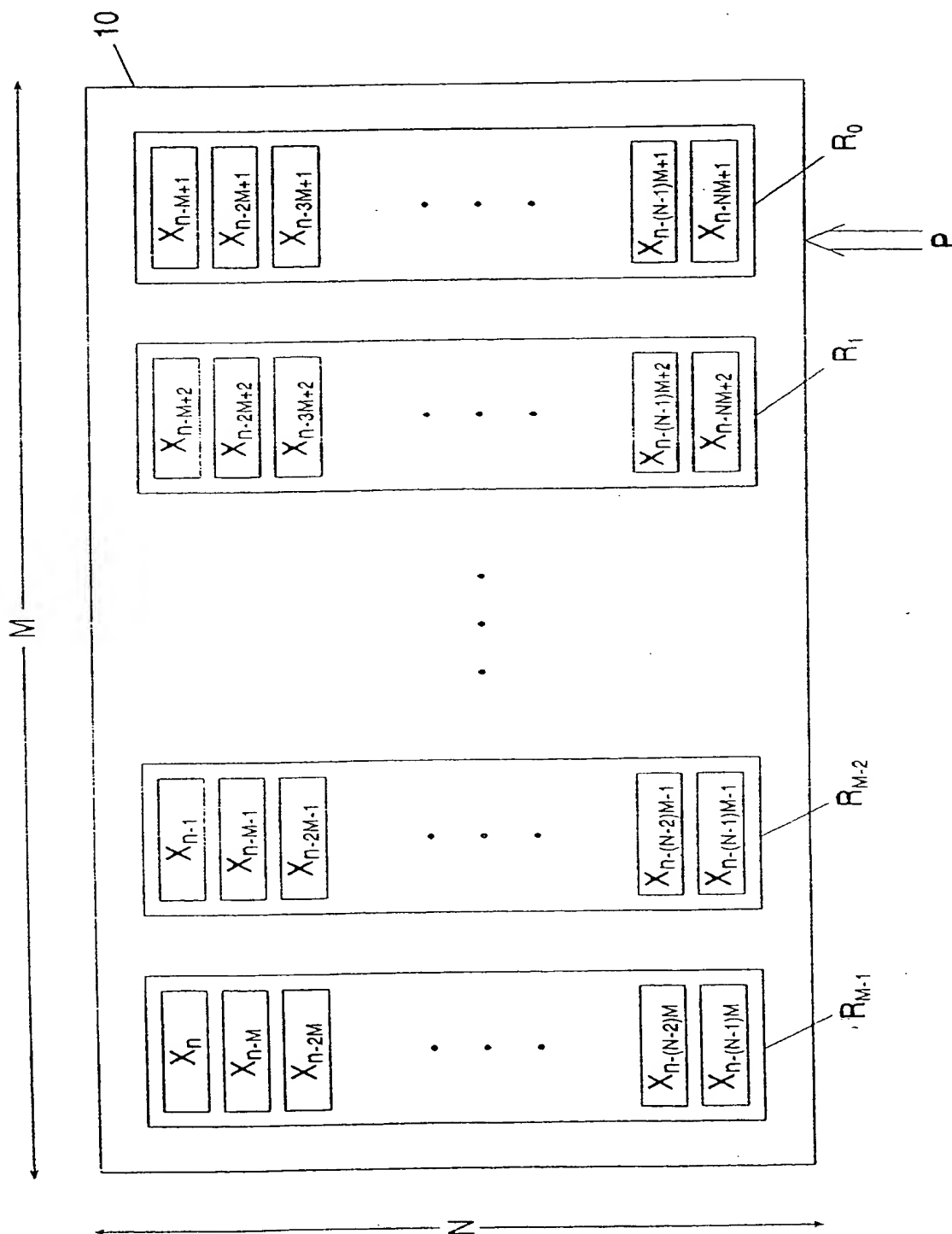


FIG. 1

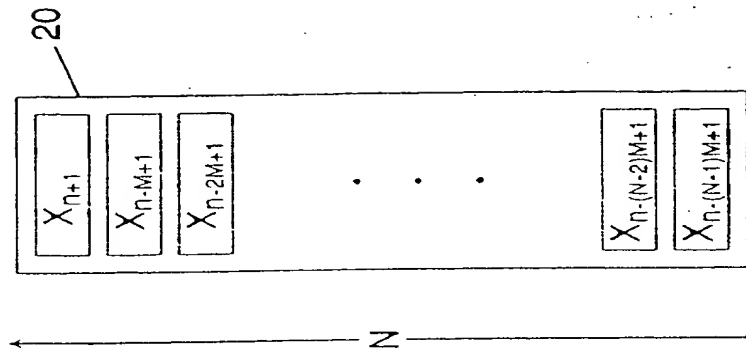


FIG. 2B

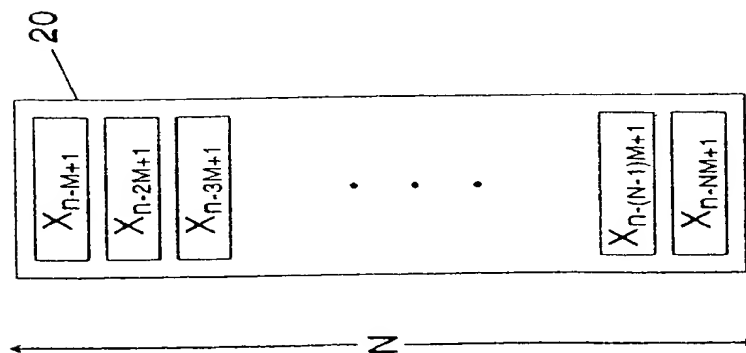


FIG. 2A

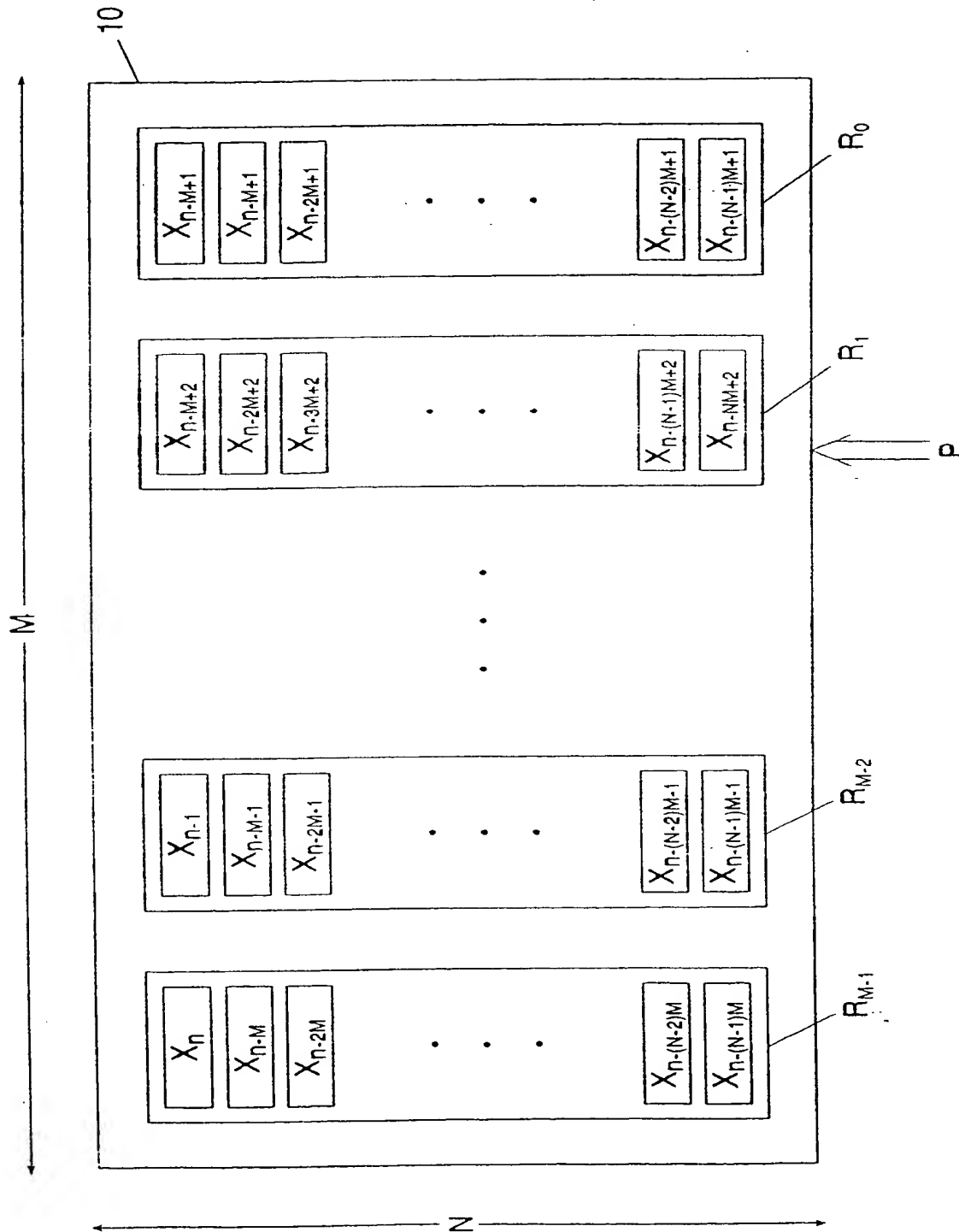


FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/19708

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : G06F 9/455

US CL : 395/500

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/500; 364/578; 327/269

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,479,128 A (JAN et al.) 26 December 1995, col. 1, lines 32-45 and Fig. 3.	1-6
Y	US 5,406,518 A (SUN et al.) 11 April 1995, Fig. 3 and col. 8, lines 20-57.	1-6

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:	* I* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
* A* document defining the general state of the art which is not considered to be of particular relevance	* X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
* E* earlier document published on or after the international filing date	* Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
* L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	* A* document member of the same patent family
* O* document referring to an oral disclosure, use, exhibition or other means	
* P* document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 25 NOVEMBER 1998	Date of mailing of the international search report 29 MAR 1999
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer KEVIN TESKA <i>Joni Hill</i> Telephone No. (703) 305-9704

WHAT IS CLAIMED IS:

1. A method of processing successive input bits, comprising the steps of:
 - (a) providing:
 - (i) a RAM having a plurality of registers, each of said registers storing a word, all of said words being of equal length,
 - (ii) a shift register at least as long as any of said words, and
 - (iii) a pointer;
 - (b) initializing said pointer to point to one of said registers of said RAM;
and
 - (c) for each group of j input bits shorter than said words:
 - (i) writing said word, stored in said register pointed to by said pointer, to said shift register,
 - (ii) shifting said word in said shift register by j bits,
 - (iii) writing said group of j input bits to said shift register, thereby producing an updated word in said shift register,
 - (iv) storing said updated word in said register pointed to by said pointer, and
 - (v) incrementing said pointer.
2. The method of claim 1, wherein j equals 1.
3. The method of claim 1, wherein all of said registers of said RAM are as long as each of said words.

4. The method of claim 1, wherein said shift register is as long as each of said words.

5. The method of claim 1, further comprising the step of:

(d) successively reading and processing at least some of said words stored in said registers of said RAM.

6. The method of claim 5, wherein all of said words stored in said registers of said RAM are read successively and processed.